Amendments to the Drawings:

The attached sheets of drawings include changes to Figs. 1-17. The changes to Figs. 1-17 include the addition of the legend "Prior Art" to Figs. 5, 6 and 10-12, and the deletion of PCT headings (e.g. 1/16, 2/16,..., and 16/16) from each of the sixteen sheets of drawings. The replacement drawing sheets submitted herewith replace the originally filed drawings and, to the best of the knowledge of the undersigned, include no new matter.

REMARKS

By the present invention, claims 1-8 and 10 have been amended, and claim 9 has been canceled. Claims 1-8 and 10 remain pending in the present application. Claims 1 and 8 are independent claims. Applicants respectfully request reconsideration and allowance in view of the foregoing amendments and the following remarks.

Objection to Title

1. The title is objected to because it is allegedly not descriptive. Applicants have changed the title from "IMPROVED TURBO DECODER" to --RECURSIVE DECODER FOR SWITCHING BETWEEN NORMALIZED AND NON-NORMALIZED PROBABILITY ESTIMATES--.

Applicants respectfully submit that the objection to the title is overcome and request withdrawal of this objection.

Objection to Drawings

2. The drawings are objected to because Figs. 5, 6 and 10-12 should allegedly be labeled by a legend such as "Prior Art" in order to clarify Applicants' invention. Applicants have amended Figs. 1-17 by adding the legend "Prior Art" to Figs. 5, 6 and 10-12, and deleting the PCT headings (e.g. 1/16, 2/16,..., and 16/16) from each of the sixteen sheets of drawings. The replacement drawing sheets submitted herewith replace the originally filed drawings and, to the best of the knowledge of the undersigned, include no new matter.

Applicants respectfully submit that the objection to the drawings is overcome and request withdrawal of this objection.

Objection to Claims

3. Claims 1-10 are objected to because of a various informalities. Applicants have amended claims 1-8, 10, and have canceled claim 9 to obviate the informalities noted on pages 2 and 3 of the Office Action.

Applicants respectfully submit that the objection to the claims is overcome and request withdrawal of this objection.

Rejection under 35 U.S.C. § 112, second paragraph

4. Claims 1 and 8 are rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. Applicants have amended claims 1 and 8, and respectfully submit that amended claims 1 and 8 meet the specific requirements of 35 U.S.C. § 112, second paragraph.

Applicants respectfully request reconsideration and withdrawal of this rejection of claims 1 and 8 under 35 U.S.C. § 112, second paragraph.

35 U.S.C. § 103(a) Rejections based on Applicants' submitted prior art and Hepler

5. Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' submitted prior art in view of Hepler (U.S. Patent No. 6,961,921 B2). The

cancellation of claim 9 renders this rejection moot with respect to this particular claim. Applicants respectfully traverse this rejection.

Amended claim 1 recites a decoder for decoding encoded data. The decoder includes a processor, normalizing means, and a switch. The processor has an input which receives probability estimates for a block of symbols, and which is arranged to calculate probability estimates for the symbols in a next iterative state. The normalizing means is for normalizing the calculated probability estimates and the normalized probability estimates. The switch is arranged to receive both the calculated probability estimates and the normalized probability estimates. An output of the switch is coupled to the input of the processor. The switch is arranged to switch between the calculated probability estimates and the normalized probability estimates depending on the iterative state.

Regarding claim 1, the Office Action fails to establish a *prima facie* case of obviousness for at least two reasons.

First, Hepler fails to teach the recited switch. The Office concedes that Applicants' submitted prior art does not disclose or reasonably suggest a switch or multiplexer coupled to a normalizer on page 5 of the Office Action. To overcome this failing, the Office states that Hepler teaches "a turbo decoder comprising a calculation stages (24 and 26) calculate alpha and normalize the alpha calculations and each alpha value is calculated on the input register (22) as well as the previously calculated alpha value provided at input (24b) and outputted from calculation stage (26) through multiplexer (28) and register (30)..."

However, Hepler does not disclose that the switch is arranged to switch between the calculated probability estimates and the normalized probability estimates depending on the iterative state, as set forth in amended claim 1. On the contrary, and referring to Fig. 3 and associated text at col. 3, lines 12-30 of Hepler, the output of the calculated probability estimate function (24) is fed directly to the normalization function (26) which normalizes the estimate before providing these to multiplexer (28). As is clearly seen in Fig. 3 of Hepler, the multiplexer (28) is not directly coupled to calculation block (24) and, as such, the switch of Hepler is not arranged to switch between the calculated probability estimates and the normalized probability estimates. Indeed, Hepler seems to have no use for the non-normalized estimates other than to normalize them prior to supplying these to multiplexer (28).

Accordingly, the Office fails to establish a *prima facie* case of obviousness and amended claim 1 is allowable over the combination of Applicants' submitted prior art and Hepler for at least a first reason.

Second, the motivation to combine Applicants' submitted prior art and Hepler is lacking. All of the claimed limitations must be taught or suggested by the prior art, and there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine the reference teachings. *In re Vaek*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Hepler teaches that the switch is used at the beginning of the calculation "to initialize the calculation and, starting at the initial state, the initial eight (8) alpha metrics are set to some

initial value, which is applied at the initialized input (28a) of multiplexer (28) in order to enable the calculation stages (24) and (26) to calculate the eight (8) values for alpha" (col. 3, lines 24-29). Thus, the teaching in Hepler of the use of the switch is for the initialization of the calculation, and this is the teaching that one of ordinary skill in the art would take from Hepler. Thus, Hepler provides no motivation for one of ordinary skill in the art to arrange the switch to receive both the calculated probability estimates and the normalized probability estimates and to switch between these depending on the iterative state, as is set forth in amended claim 1. Thus, notwithstanding the fact that the combination of prior art applied by the Office fails to disclose, teach, or reasonably suggest the features of amended claim 1, one of ordinary skill in the art simply has no motivation to make this combination.

Therefore, amended claim 1 is allowable over the combination of Applicants' submitted prior art and Hepler for at least a second reason because Applicants' submitted prior art, Hepler, or any combination thereof, provides no motivation whatsoever to modify the teachings thereof to provide the limitations set forth in amended claim 1.

Claims 2-7 are allowable as being dependent from an allowable claim.

Amended claim 8 recites a decoder for decoding encoded data. The decoder includes a processor, normalizing means, pipelining means, and switching means. The processor has an input which receives probability estimates for a block of symbols, and which is arranged to calculate probability estimates for the symbols in a next iterative state. The normalizing means is coupled to the processor for normalizing the calculated probability estimates to provide

normalized probability estimates. The pipelining means is between the processor and the normalizing means for providing non-normalized probability estimates. The switching means is for receiving both the calculated probability estimates and the normalized probability estimates. An output of the switching means is coupled to the input of the processor. The switching means is arranged to switch between the calculated probability estimates and the normalized probability estimates depending on the iterative state.

Claim 8 is allowable for reasons analagous to those given for claim 1.

Claim 10 is allowable as being dependent from an allowable claim.

Applicants respectfully request reconsideration and withdrawal of the rejection of Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Applicants' submitted prior art in view of Hepler.

Conclusion

5. All of the stated grounds of rejection have been properly traversed. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections, and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

No additional fees are believed to be required. However, if the Office deems that any fees are necessary, authorization is hereby granted to charge any required fees to Deposit Account No. 22-0261.

Prompt and favorable consideration of this Amendment is respectfully requested.

April 10, 2006

Respectfully submitted,

By 

Michael A. Sartori, Ph.D.
Registration No. 41,289
Thomas C. Schoeffler
Registration No. 43,385
VENABLE LLP
P.O. Box 34385
Washington, DC 20043-9998
Telephone: (202) 344-4000
Telefax: (202) 344-8300
Attorney/Agent for Applicant

MAS/TCS

Appl. No. **10/649,785**
Art Unit **2133**
Customer No. **26694**
Confirmation No. **5599**
Annotated Sheet Showing Changes

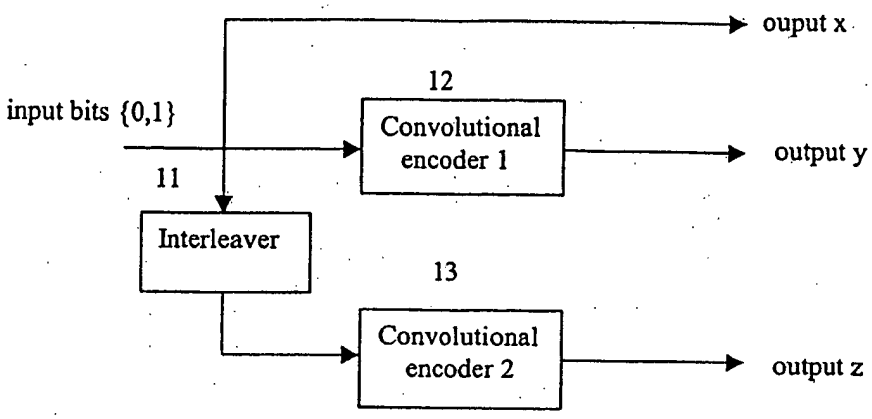


Figure 1 Basic Architecture of Turbo Encoder (Coding Rate = 1/3)

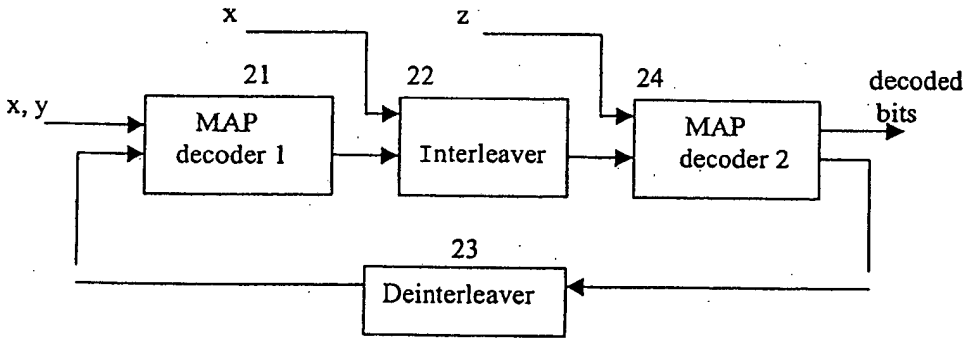


Figure 2 Basic Architecture of Turbo Decoder (Coding Rate = 1/3)

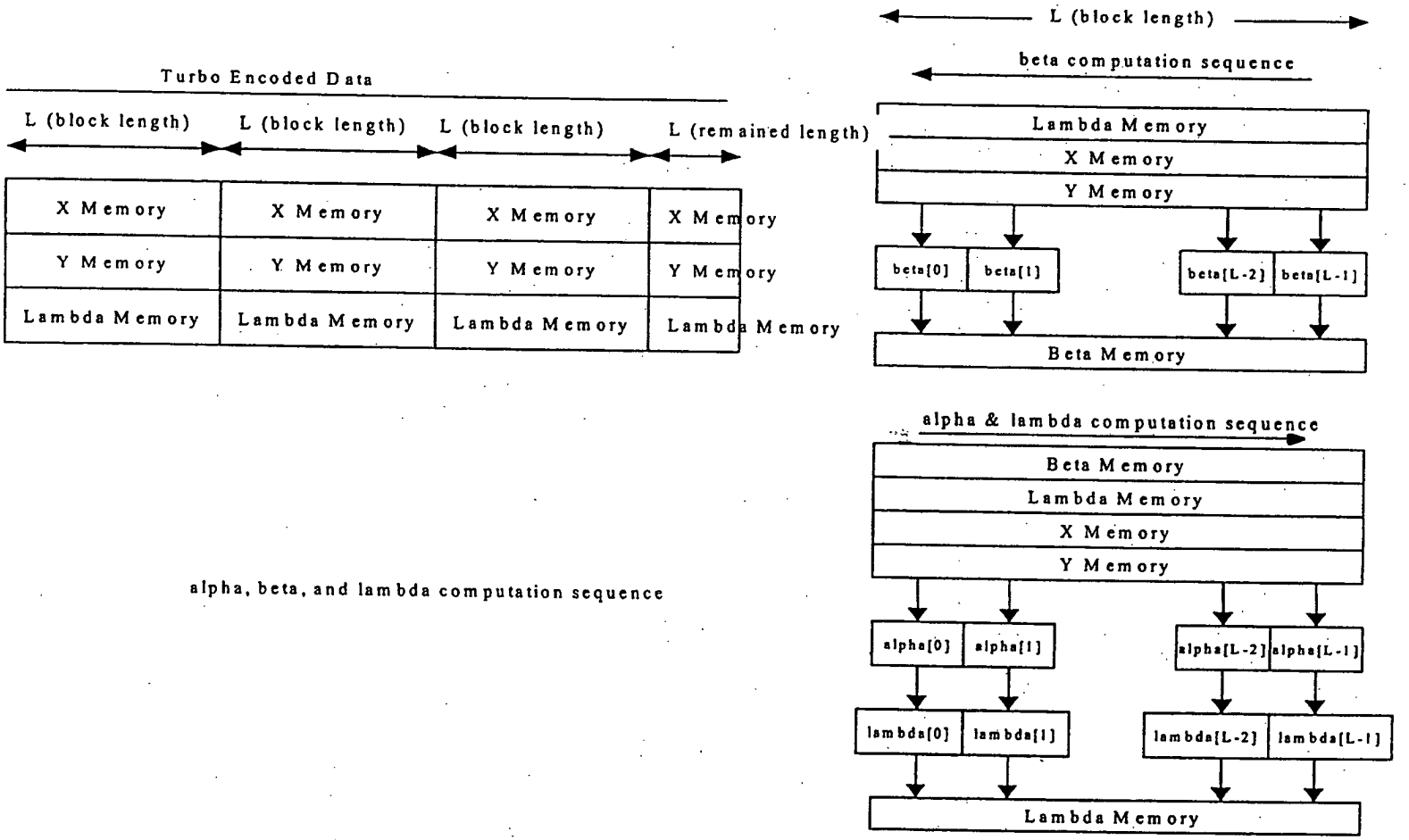


Figure 3. Alpha, Beta and Lambda Calculation Sequence

State Transition in Beta Computation

State m	0	1	2	3	4	5	6	7
Next[m][0]	0	4	5	1	2	6	7	3
Next[m][1]	4	0	1	5	6	2	3	7

State Transition in Alpha Computation

State m	0	1	2	3	4	5	6	7
prev[m][0]	0	3	4	7	1	2	5	6
prev[m][1]	1	2	5	6	0	3	4	7

Figure 4 State Transition in Beta and Alpha Computation.

Appl. No. 10/649,785
Art Unit 2133
Customer No. 26694
Confirmation No. 5599
Annotated Sheet Showing Changes

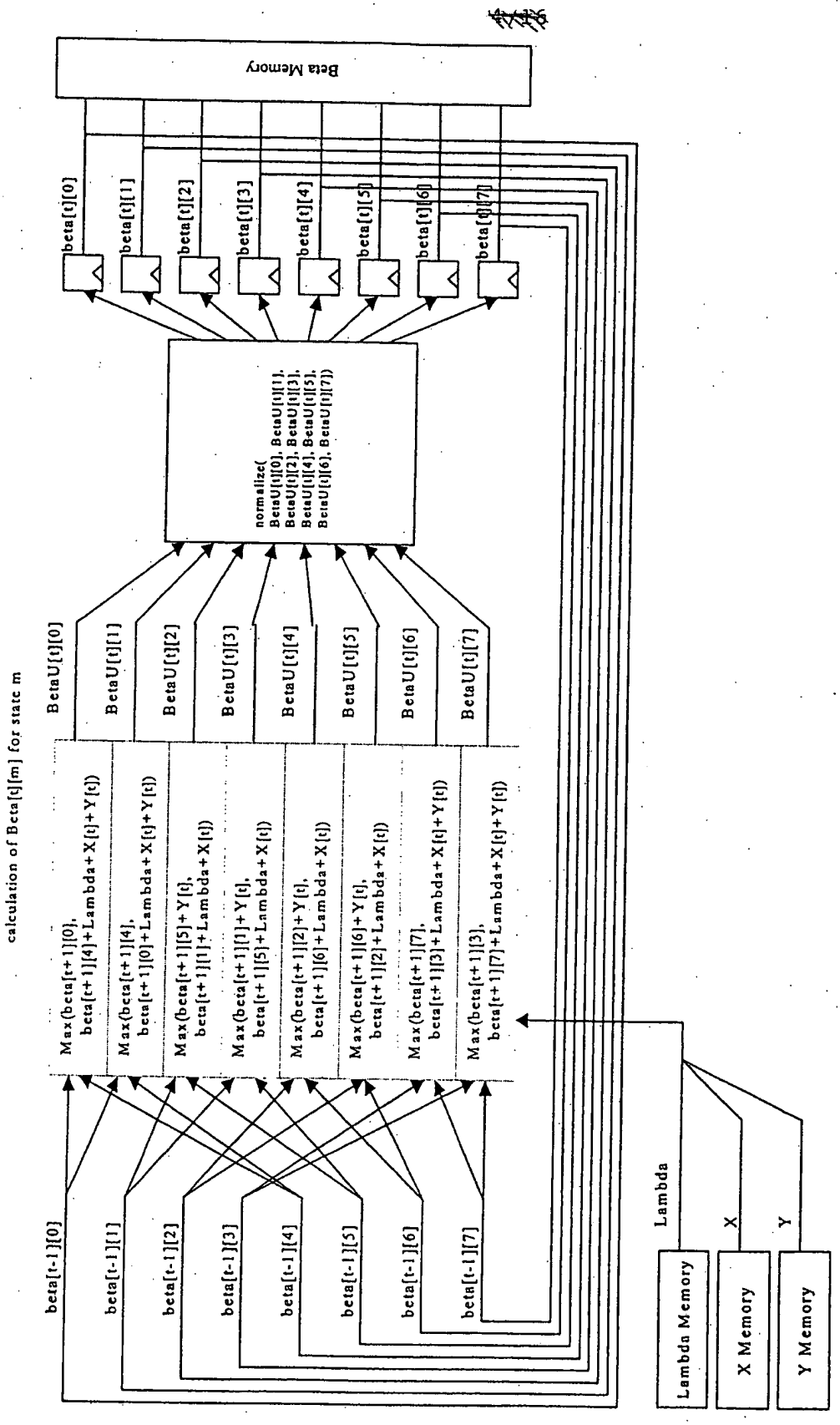


Figure 5. Beta Computation Block Diagram

Prior Art

~~FIG. 6~~

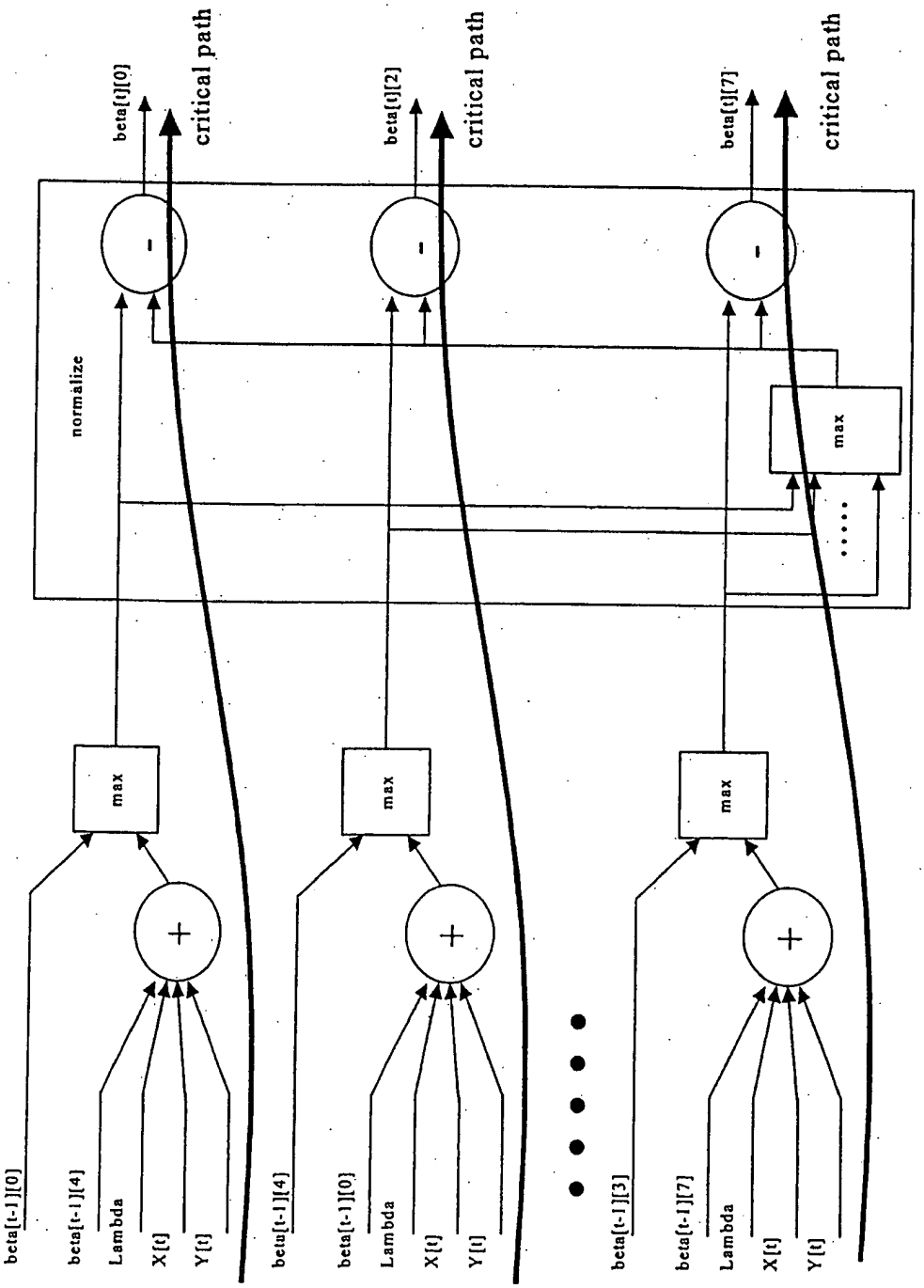


Figure 6 Details Beta Computation and Critical Path Block Diagram

Prior Art

~~616~~

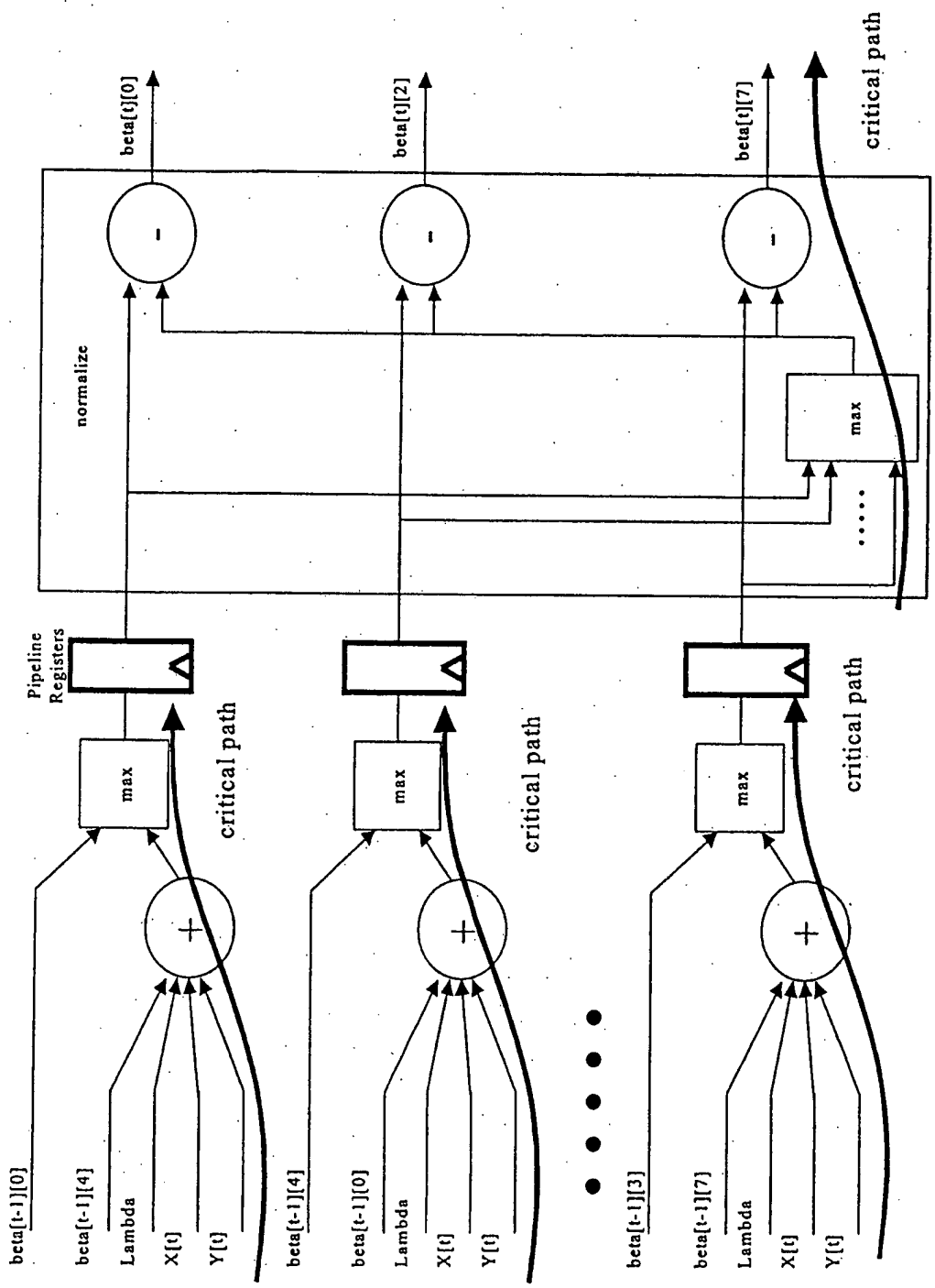


Figure 7: The Improved Structure of Beta Computation and Critical Path Diagram

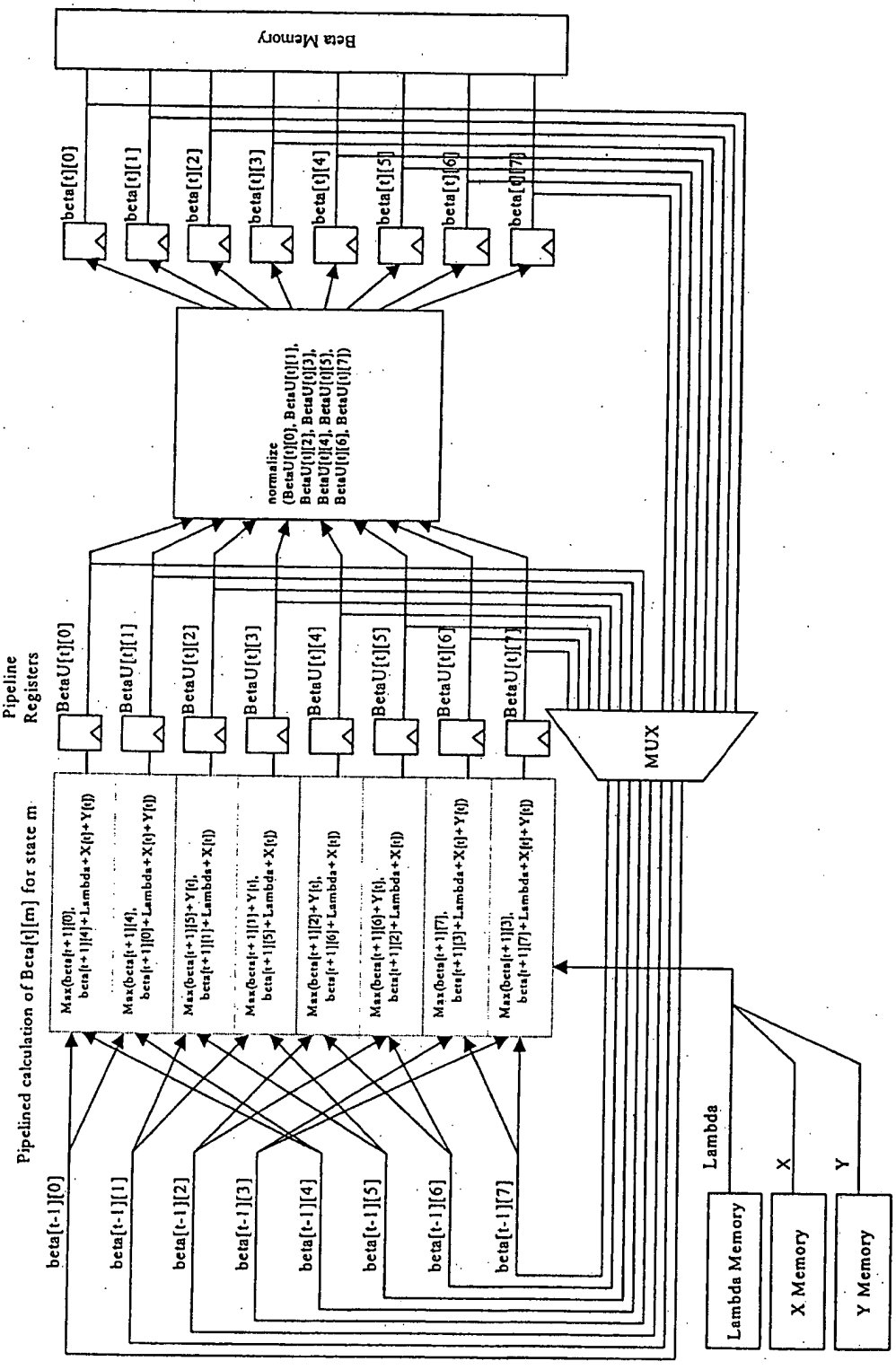


Figure 8 Overall Structure of Pipelined Beta Computation Path Diagram

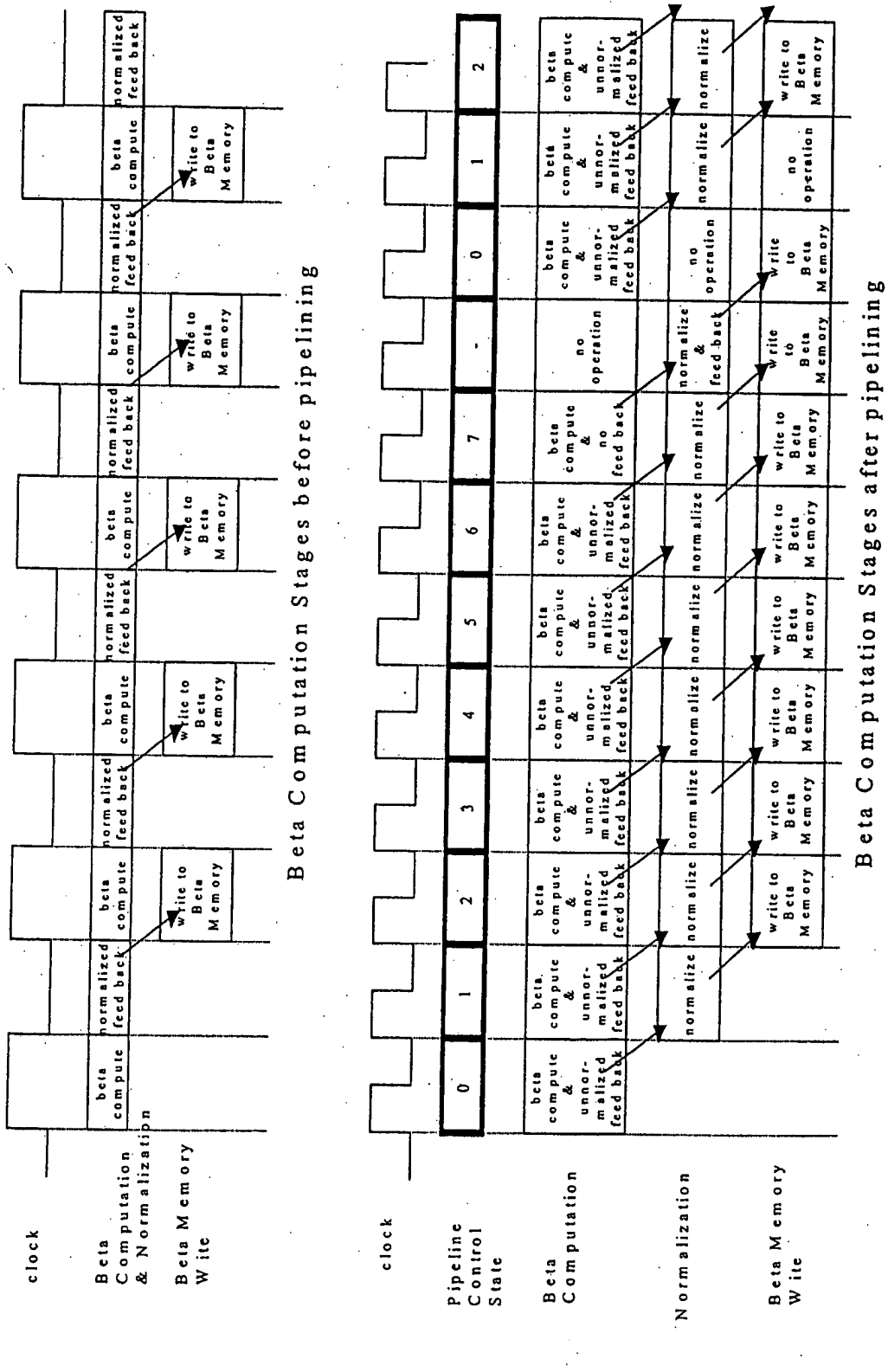


Figure 9 The pipeline Stages of Beta Computation Diagram

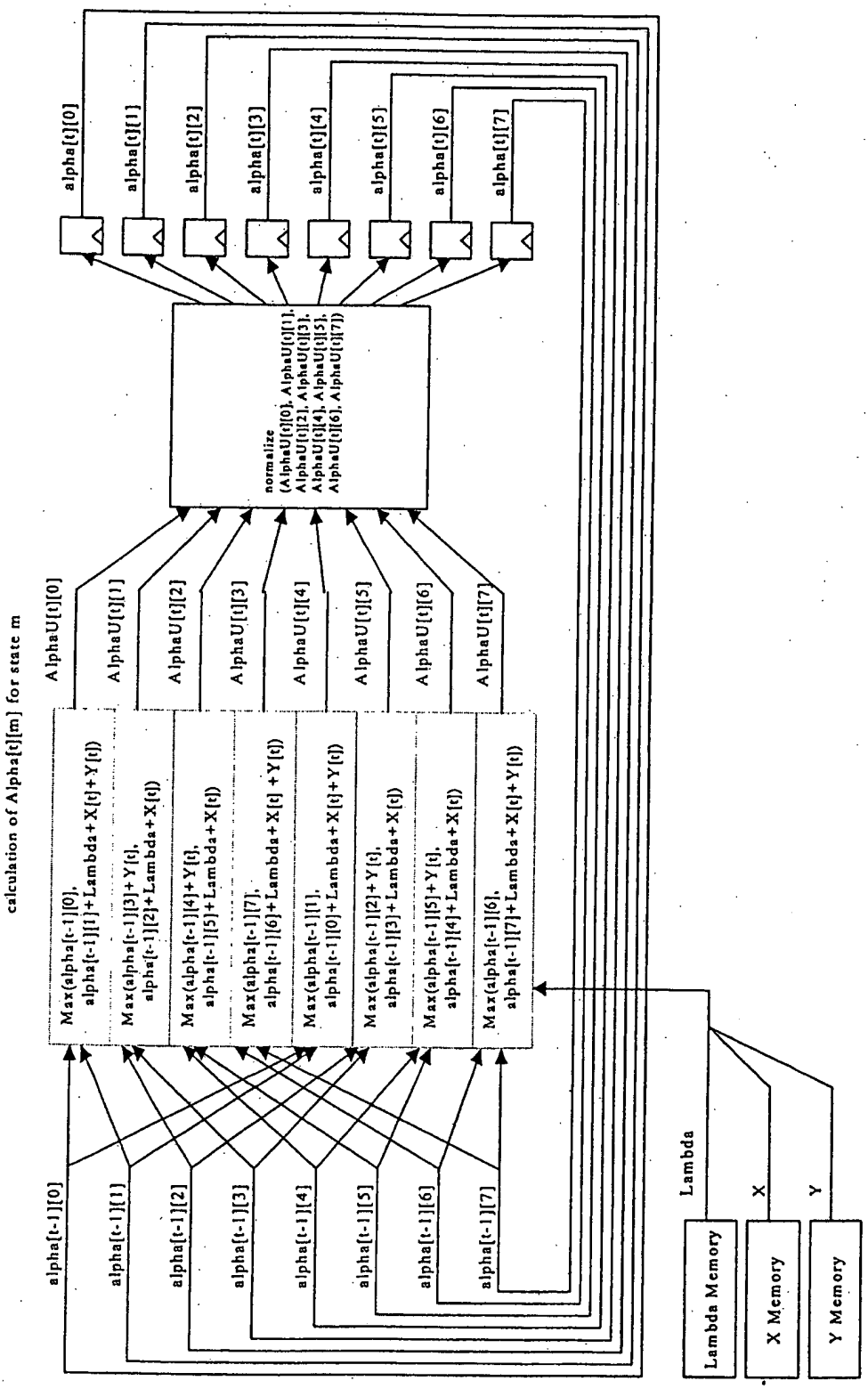
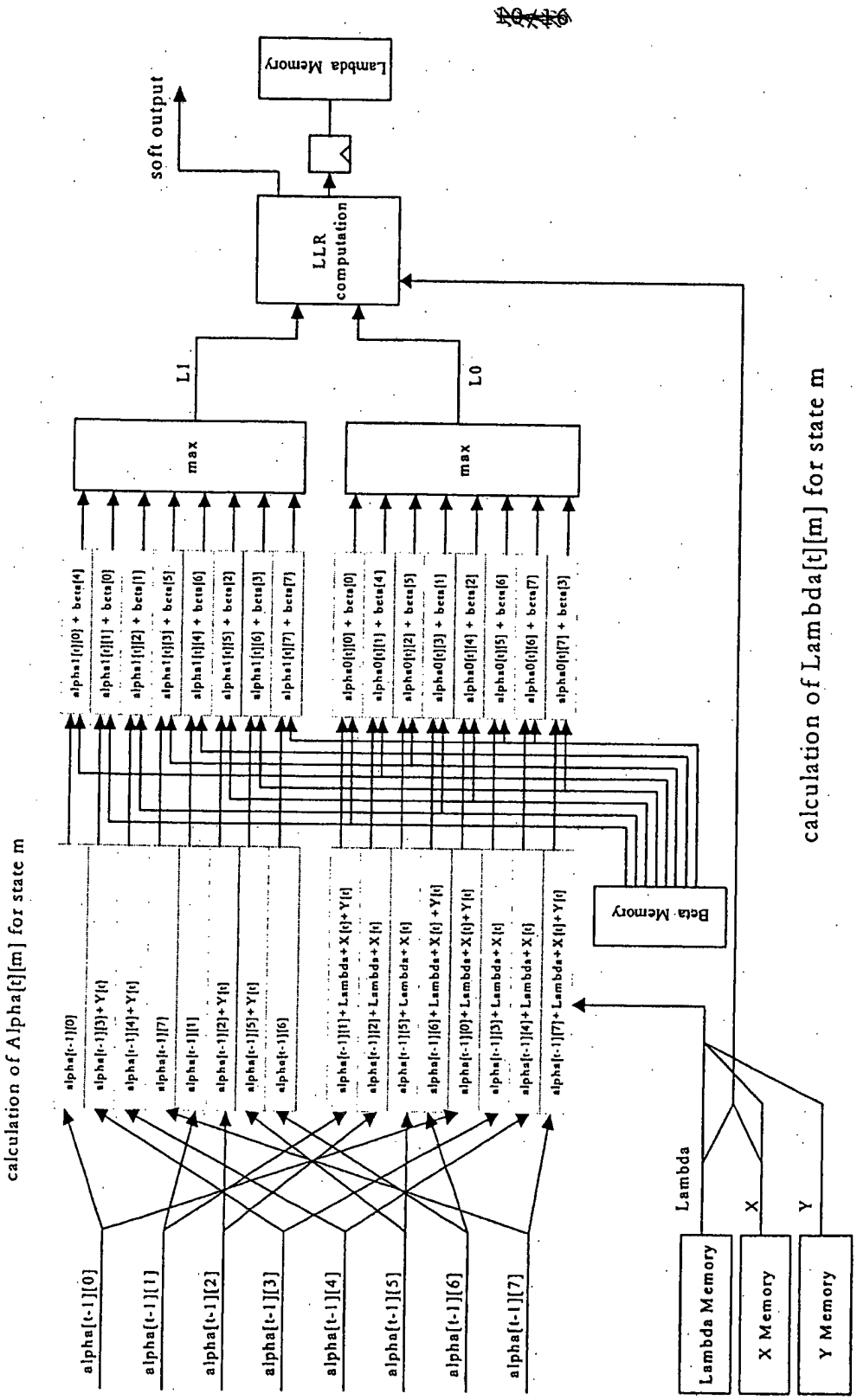


Figure 10 Alpha Computation Block Digram

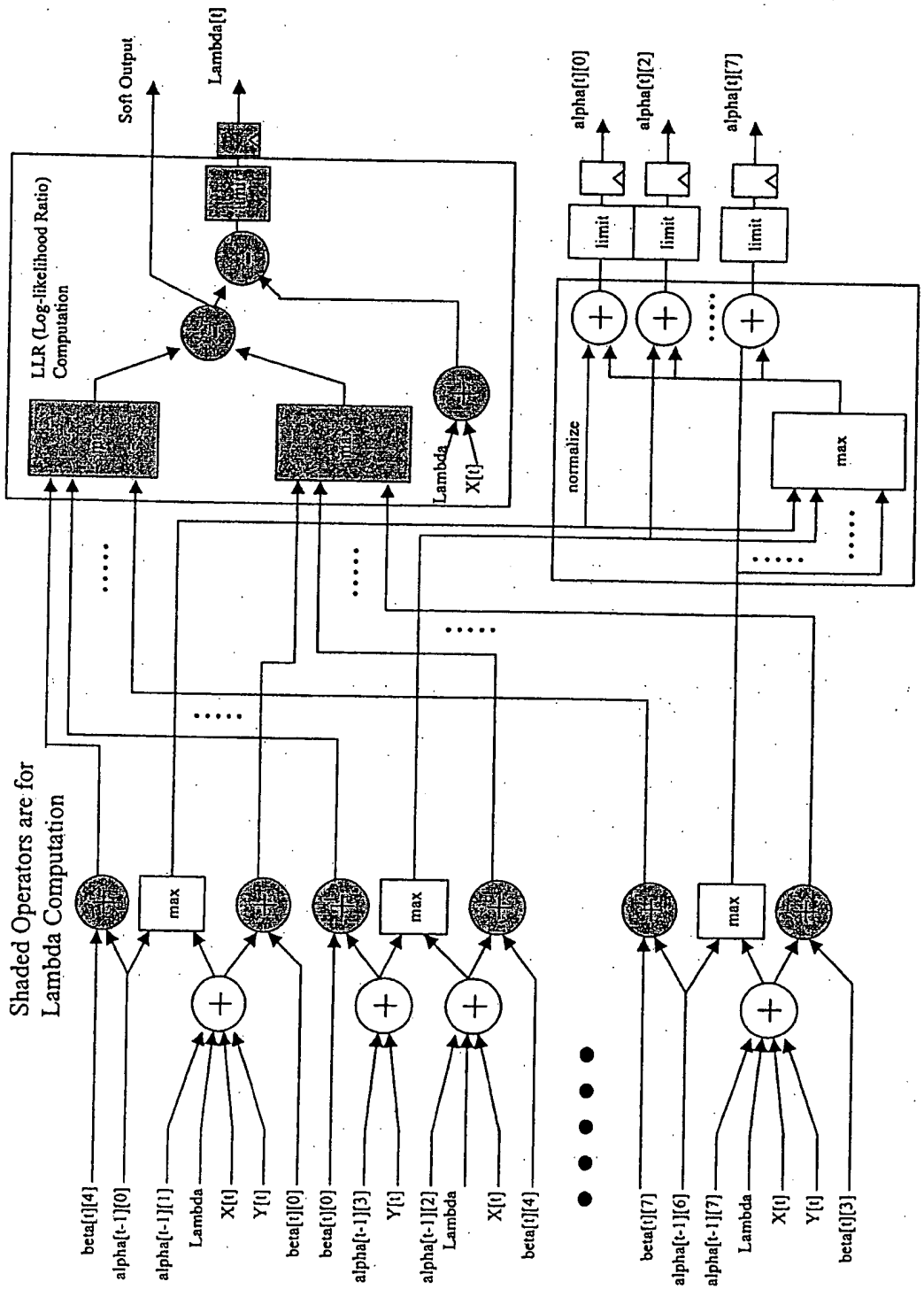
Prior Art



Prior Art

Figure 11 Lambda Computation Block Diagram

~~Fig. 6~~



Prior Art

Figure 12 Details Alpha and Lambda Computation and Critical Path Block Diagram

~~12/16~~

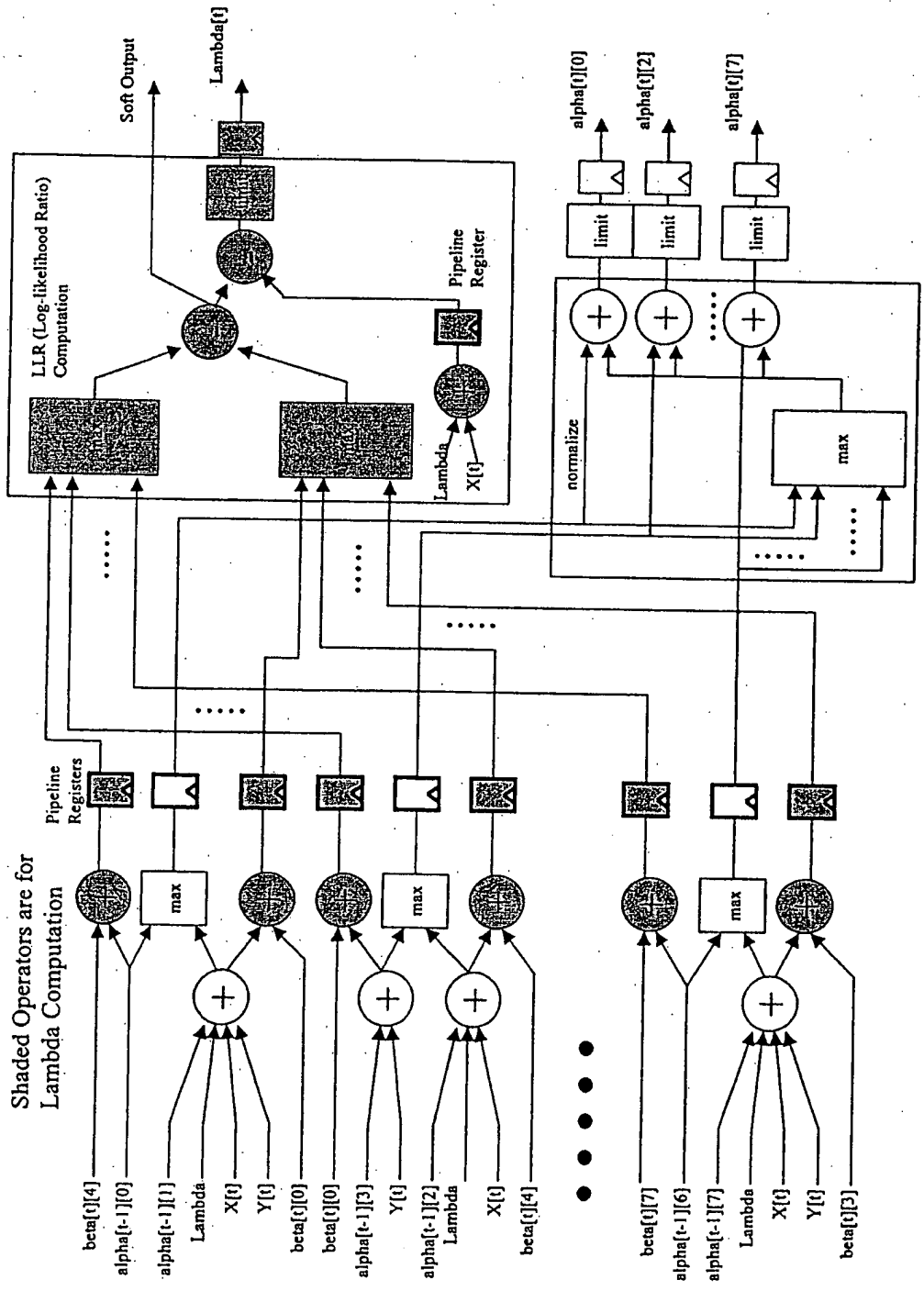


Figure 13 Improved Structure of Alpha and Lambda Computation and Critical Path Diagram

~~12/16~~

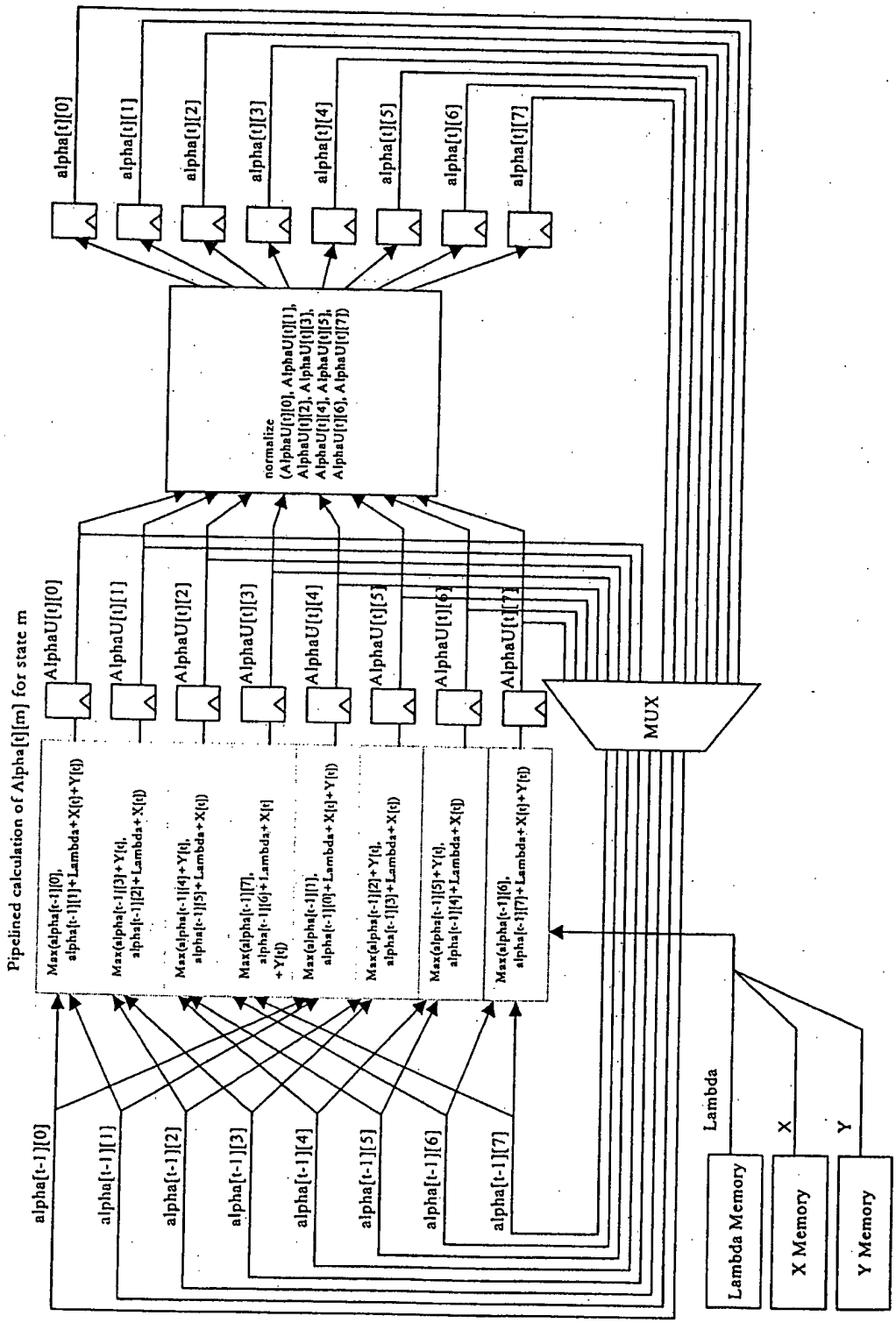


Figure 14 The Overall Structure of Pipelined Alpha Computation Path Diagram

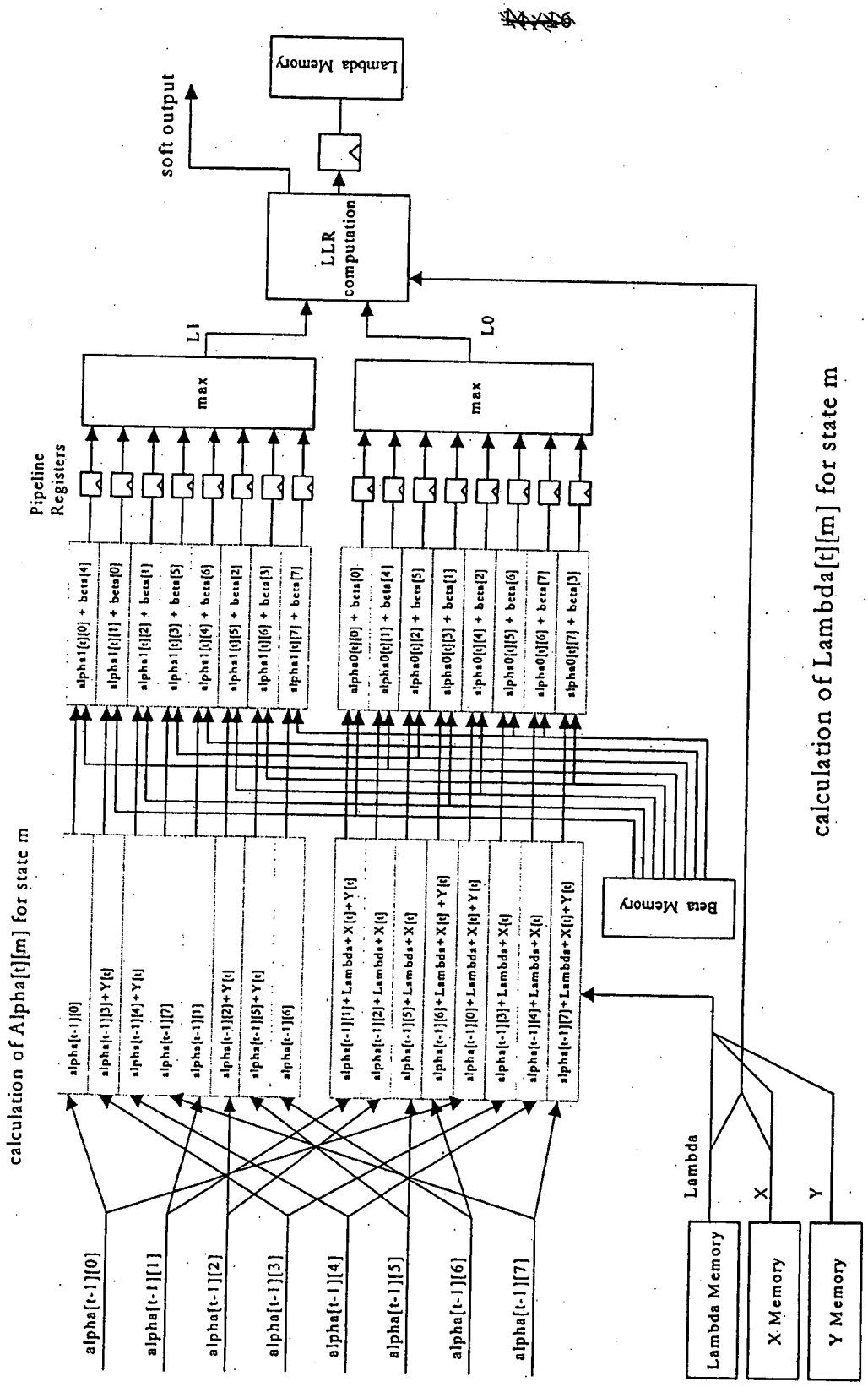


Figure 15 The Overall Structure of Pipelined Lambda Computation Path Diagram

~~FIG. 16~~

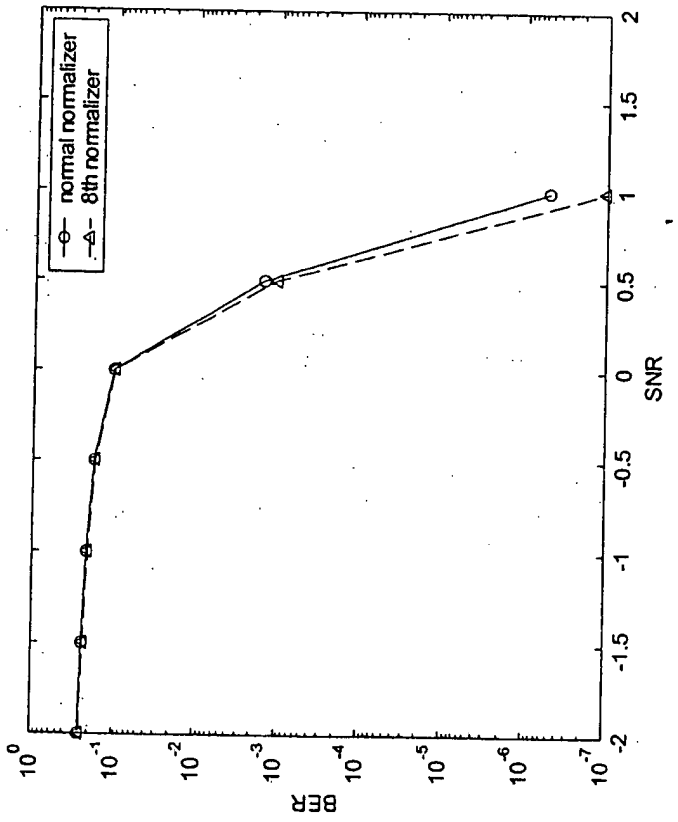


Figure 16 BER and SNR simulation for original normalization and new normalization
Block length = 3856 bits)

~~16/16~~

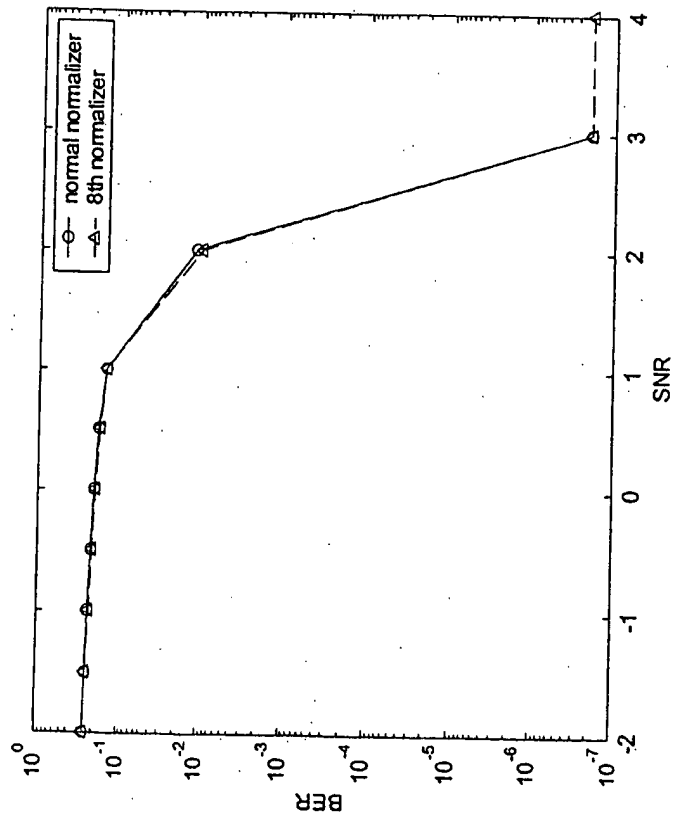


Figure 17 BER and SNR simulation for original normalization and new normalization (Block length = 5114 bits)